

PRODUCT BRIEF

SensIR™ Multiplexer Integrated Circuit

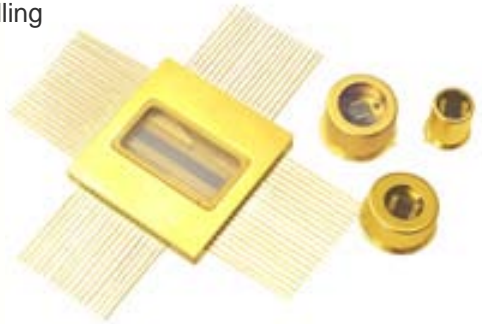
Advantages

- New Automated Chemical Processing (ACP) produces higher yield at lower cost.
- Extremely high reliability under extreme conditions.
- Long shelf life.
- Hermetically sealed package to completely eliminate humidity attack on detection area.
- Wide range of electrical characteristics available.
- Wide range of sizes available.
- Immediate delivery.
- Compact integrated filter/detector combinations.
- 100% tested.
- State of the art microelectronics fabrication capability.
- Specializing in high density arrays.

Overview

The SensIR™ multiplexer (“mux”) IC performs all functions of detector array interface, signal processor and readout device for the SensIR™ focal plane array. With each mux IC controlling 32 detector channels, array architecture is modular and expandable.

Input/Output pins are provided for data output, power and control. (See below.)



Mux Operation

The channel cell input is a cascade configuration where the detector current branches into three parts. There are two skimming branches and one signal branch. There is one global skim which draws equal currents for all channels. The other skimmer provides independent adjustment for each channel by use of a local 6 bit digital to analog converter controlled by a static memory. This local skim permits correction of level non-uniformities between detector channels.

The local memory is loaded by a serial data line and may be loaded at power up or “on the fly” dynamically during the readout cycle. After skimming, the remaining signal current is time integrated by charging a capacitor. The size of the capacitor is selectable for values of 1, 4, 7, or 10 pF. The integration time is controlled by an externally applied Integration Clock. Two internal cell control signals, “RST” and “SAMP”, are derived from the Integration Clock.

Multiplexer readout timing uses only two control signals. “FRAME START” begins the readout cycle. Then with each “PIXEL CLOCK” the multiplexer address is incremented by one. After 32 clock cycles all channels in one chip have been enabled, one at a time. Several chips may be cascaded by connecting “SHIFT REGISTER OUT” to the “FRAME START” of the following chip. There is a Channel 1 buffered output permitting user timing generation and synchronization.

The local skim is controlled with a serial data input which loads the local static memory. Data is clocked in by the “DAC INPUT CLOCK” and is shifted into the DAC register on the rising edge of “DAC LOAD ENABLE”. The high and low reference voltages for the DAC are brought out of the chip to allow the user to control the granularity of the local skim.



Input/Output PINS

The typical room temperature response for PbSe operates in the 1.0 to 4.5 micron spectral region with time constants below 2 μ sec. TE-cooled packages are available with a response in the 1.0 to 5.0 micron region with increased D*.

VDD (2 Pins) - Power, typically 5-7V

VSS (2 Pins) - Ground

FRAME START - This is a pulse, one PIXEL CLK wide, to initiate the read-out sequence.

CHANNEL 1 OUTPUT - Output to indicate Channel 1 output time period

TE COOLER (+) - Positive terminal for thermoelectric cooler

TE COOLER (-) - Negative terminal for thermoelectric cooler

THERMISTOR 1 (2 Pins) - Thermistor bead for TE cooling, nominally 3 Kohms at 0°C

THERMISTOR 2 (2 Pins) - Thermistor bead for TE cooling, nominally 3 Kohms at 0°C

DETECTOR BIAS - Positive bias voltage with respect to VDD, for detectors

ANALOG MUX OUTPUT - Muxed data output Line

DAC V LO - Minimum DAC voltage level. DAC Value = 0

GLOBAL SKIM - Analog voltage input which controls global skim setting

DAC V HI - Maximum DAC voltage level. DAC Value = 31

SHIFT REGISTER OUTPUT - This line indicates the last channel is connected to the MUX DATA OUTPUT. This line may be used for external circuits or for cascading to the INTEGRATION CLOCK line of the following chip in a multiple chip application.

WELL CAP SELECTION - Both low provide a minimum well capacitance of 1pF. 3 PF WELL SELECT - High level adds 3pF 6pF WELL SELECT - High level adds 6pF.

INTEGRATION CLOCK - Sets the period of integration for all channels. Clock "high" time period sets the integration time. Clock "low" time provides the data sample-and reset periods.

DAC DATA - A single serial input data line provides input data to an internal serial-to parallel converter which, in turn, feeds the DAC control coefficients to the channel RAM memory.

DAC INPUT CLOCK - This input clocks the serial DAC input into the serial-to-parallel register. Input data is clocked on the rising edge of this input.

DAC LOAD ENABLE - This input clocks the enable which allows the DAC data to be latched into the channel RAM during the channel address readout time period. Data is loaded on the low to high transition of the DAC LOAD EN line, during the particular channel address readout time period.

MUX READOUT CLOCK - This clock controls the data readout rate.



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Power Supplies

The four power and bias voltages (VDD, DAC HI, DAC LO, G SKIM) must be low noise and should be filtered with a small tantalum (10uF) capacitor to ground (VSS). Noise and drift on these voltages appears in the channel outputs. This effect is larger for larger integration times and smaller well capacitors. If the bias voltages (DAC HI, DAC LO, G SKIM) are not used they must be connected to ground (VSS).

Well Size

The nominal well capacitance is 1pF, and with a 7V supply a maximum output of 5V is possible. When using either of the programmable well capacitors (3pF or 6pF) the maximum output voltage of 5V may still be achieved when using a 7V supply.

Integration Time

The minimum integration time is 10 μ s, while the maximum integration time should be >100ms with proper use of the global and DAC skim.

Global Skim

The Global Skim input is connected to the gate of identical current skim transistors, one for each channel. The nominal range of the Global Skim voltage is:

0.8 to 1.2 V at room temperature

0.9 to 1.2 V at cryogenic temperatures

DAC Voltages

The voltages, DAC HI and DAC LO, set the upper and lower limits of the DAC output. The difference between these voltages should be kept as small as possible while still compensating for the non-uniformities among the channels. A difference in the range of 0.1 to 0.2 Volts is typical.

Notes

1. No connection should be made to any pad locations not specifically listed above.
2. Maximum values: VDD 10 VDC (6-7 VDC recommended)
Clock 2 MHz
3. All user-accessible inputs and outputs have built in ESD protection. However the mux is CMOS and proper ESD procedures should be followed when handling the focal plane array.



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