

10-bit MEMS Photonic Time Delay with Variable Optical Attenuator

(Protected by US Patent 10752492B2)

Product Description

The MEMS Series Photonic Time Delay digitally varies the optical delay time in fiber by selectively routing optical signal through N fiber loops whose lengths increase successively by a power 2 of the increment time delay ΔT . Since each switching element allows the signal to either pass or bypass a fiber loop, a delay T may be inserted, which can take any value (in increments of ΔT) up to the maximum value $[T = (2^N-1)\Delta T]$.

This is achieved using a patent pending MEMS switching configuration and activated via an direct DC electrical control signal.

The driver is available with USB or

The driver is available with USB or RS232 control interface separately.



Performance Specifications

Min	Typical	Max	Unit		
780	1550	2000	nm		
		10	Loop		
	1.2	2.0 [1]	dB		
	0.1	0.2	dB		
18	24		dB		
40	50		dB		
50	55		dB		
	2	10	ms		
4		10			
		10	ms		
	0.1	0.2	ps		
-5		70	°C		
-40		85	°C		
	300		mW		
44L	44L x 15.5W x 6.5H				
	780 18 40 50 4 -5 -40	780 1550 1.2 0.1 18 24 40 50 50 55 2 4 0.1 -5 -40 300	780 1550 2000 10 1.2 2.0 [1] 0.1 0.2 18 18 24 40 50 50 55 2 10 4 10 10 0.1 0.2 -5 -40 85 300		

- [1]. Input to output with a single delay (1 m fiber length) loop.
- [2]. The delay fiber loops (>0.5m) can be spliced in precise length control per request.

Features

- . 10-bit Resolution or more
- . High Reliability
- · Low Insertion Loss

Applications

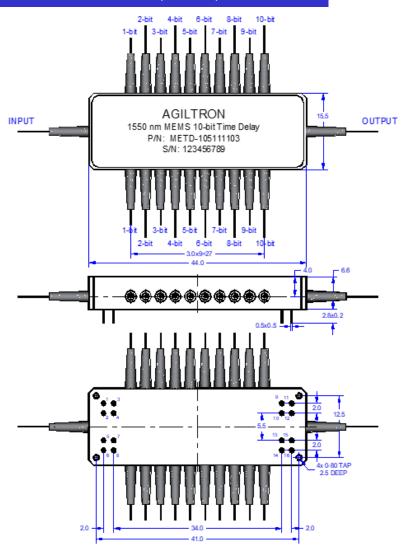
- · Phase-Array Antennas
- Instrumentation





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Mechanical Dimensions (Unit: mm)



^{*}Product dimensions may change without notice. This is sometimes required for non-standard specifications.

Electrical Driving Requirements

The electrical driver is available with USB or RS232 control interfaces and Windows™ GUI. It comes with a wall-plug 5V power supply. Please contact us it.

Driving Voltage	Min	Typical	Max	Unit
Н	4.6	4.8	5.0	VDC
Power Consumption (For each MEMS Chip)		170		mW

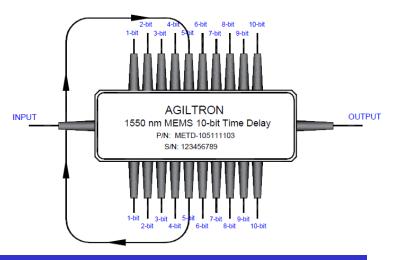




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Status		Pin Number											
	1	2	3	4	5	9	10	11	12	13	6, 7, 8, 14, 15, 16		
Bypass													
1-bit	Н												
2-bit		Н											
3-bit			Н										
4-bit				Н									
5-bit					Н						0V		
6-bit						Н							
7-bit							Н						
8-bit								Н					
9-bit									Н				
10-bit										Н			

Delay Path Definition: ex. 5th-bit path diagram



Ordering Information

METD ^[1] -				2			0	
	Туре	Wavelength Configuration [2]		Package	Fiber Type		Delay Range	Connector
	4-Bit = 04 5-Bit = 05 6-Bit = 06 7-Bit = 07 8-Bit = 08 9-Bit = 09 10-Bit = 10 Special=00	1260-1620 =1 1310=3 1550=5 Special=0	TD only =1 TD & VOA =2 Special = 0	Non- Latching=2 Special =0		Bare fiber=1 900 µm tube =3 Special =0	Custom =0	None =1 FC/PC =2 FC/APC =3 SC/PC =4 SC/APC =5 ST/PC =6 LC =7 Duplex LC=8 Special=0



^{[2].} TD: Time Delay. VOA function may be realized in the additional PIN (not shown in driving table).

